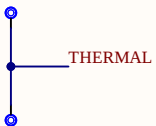
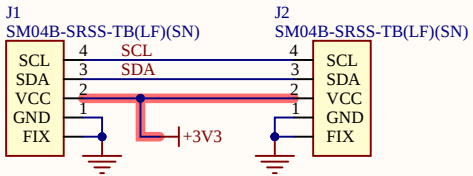


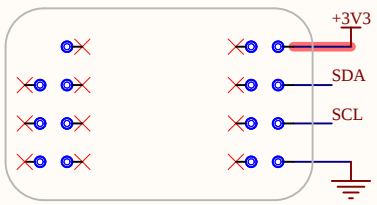
I2C ADDRESS 0x44



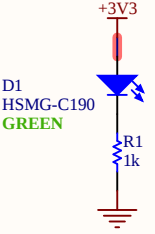
I2C CONNECTORS



TEST POINTS
BOTTOM VIEW



POWER
LED



Fiducial_1
Fiducial mark 1mm

Fiducial_2
Fiducial mark 1mm

Fiducial_3
Fiducial mark 1mm

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Title: TOP

ID: ABX00103

Version: V0.3

Date: 27/06/2024 Time: 16:16:44

Sheet 1 of 1

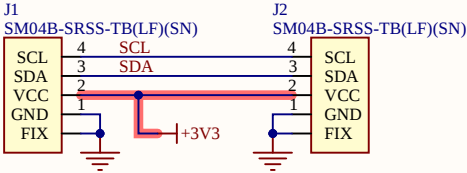
File: TOP.SchDoc

Author: Silvio Navaretti

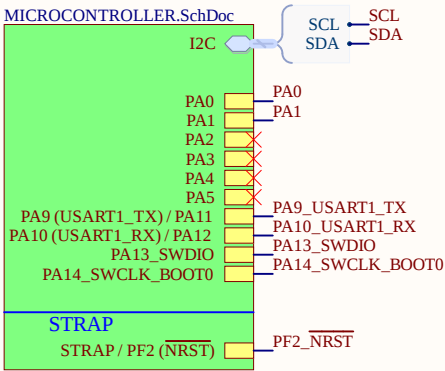
RevAuthor: Silvio Navaretti



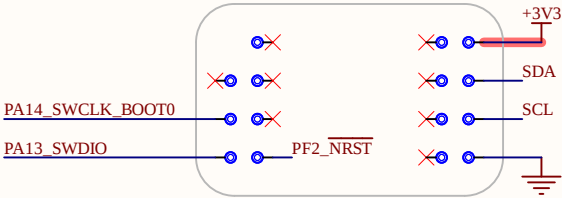
I2C CONNECTORS



MICROCONTROLLER



TEST POINTS
BOTTOM VIEW



POWER
LED



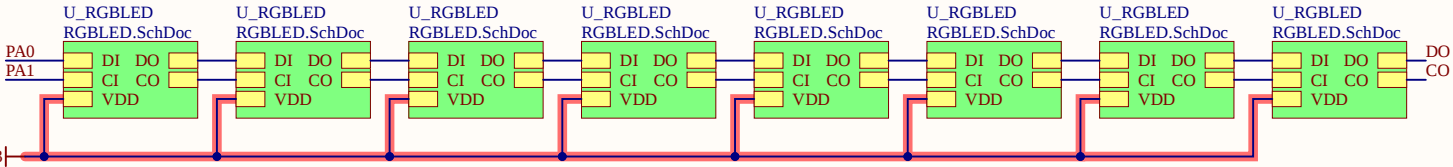
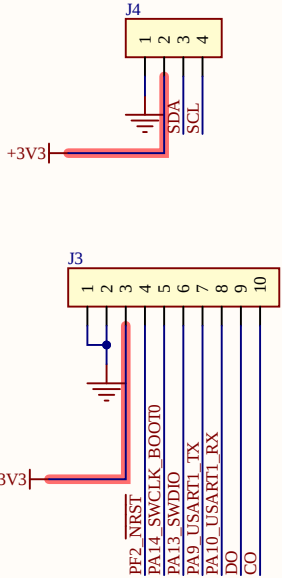
QR1
QR CODE 4x4mm



Fiducial_1
Fiducial mark 1mm

Fiducial_2
Fiducial mark 1mm

Fiducial_3
Fiducial mark 1mm



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ID: **ABX00109**

Date: **27/06/2024** Time: **16:25:11**

File: **TOP.SchDoc**

Version: **V0.3**

Sheet **1** of **3**

Author: **Silvio Navaretti**

RevAuthor: **Silvio Navaretti**

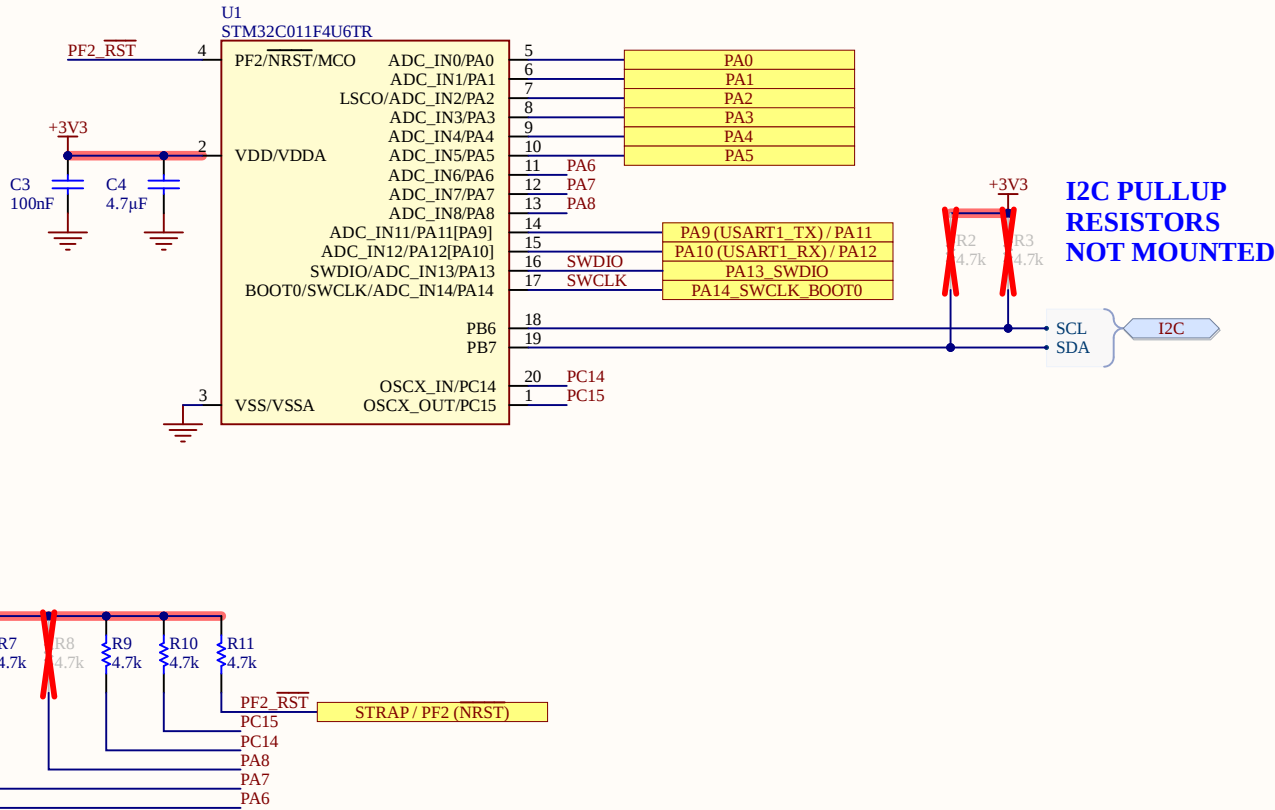


Table 11. Terms and symbols used in Table 12		
Column	Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
I/O structure		Options for FT I/Os
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function

Table 12. Pin assignment and description

Pin	Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
20	PC14- OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
1	PC15- OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMB, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.



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ID: ABX00109

Date: 27/06/2024 Time: 16:25:12

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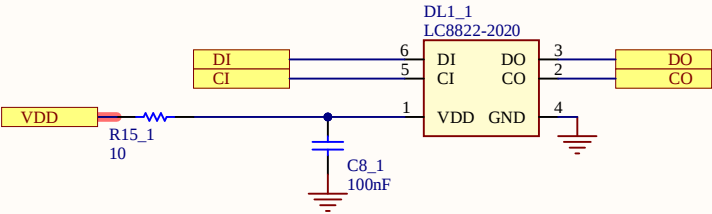
Version: V0.3

Sheet 2 of 3

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti



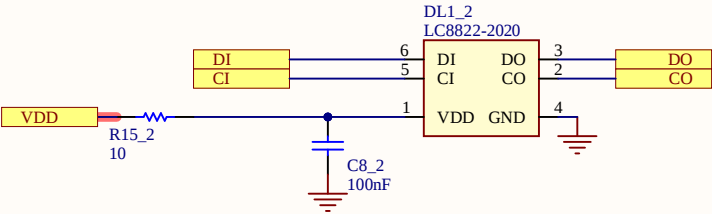


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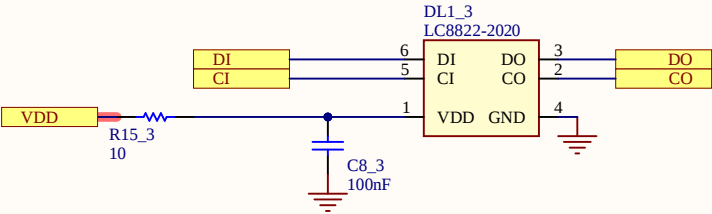


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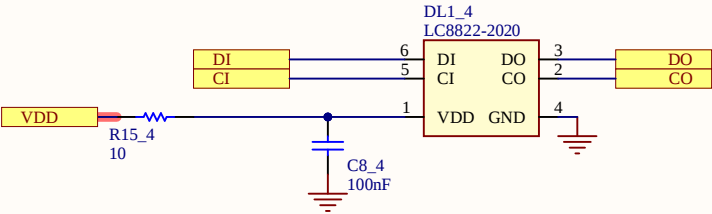


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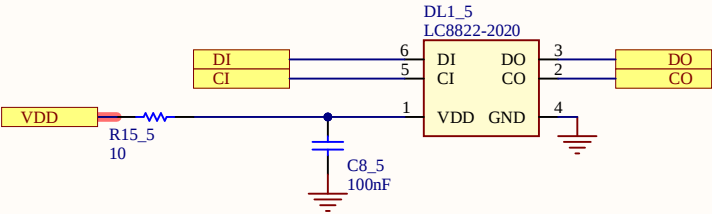


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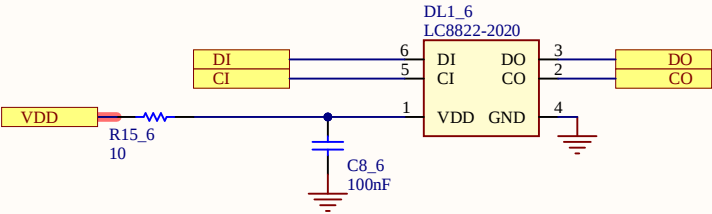


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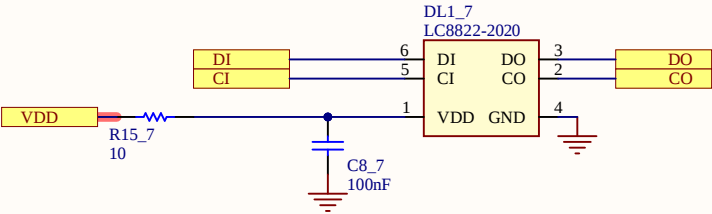


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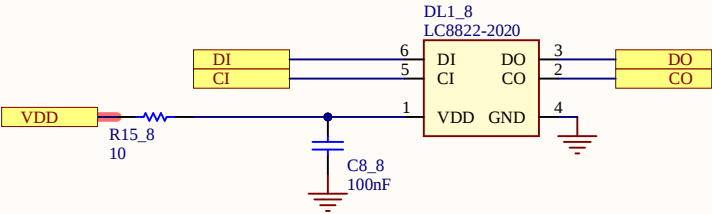
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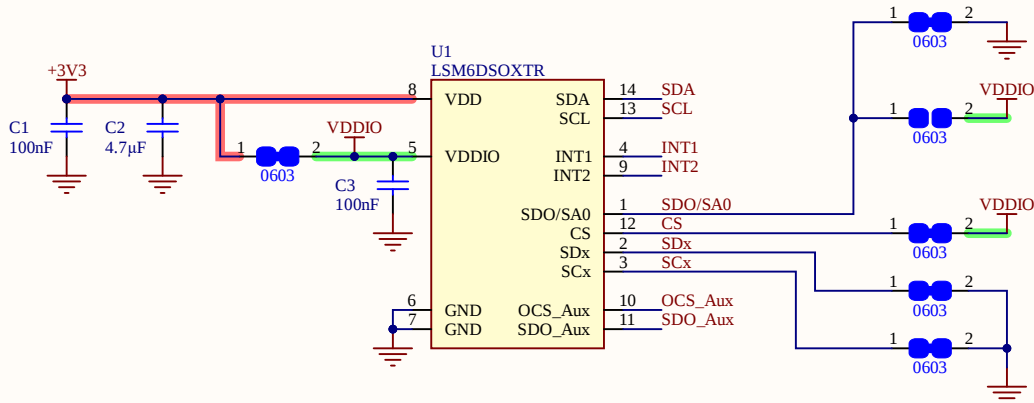


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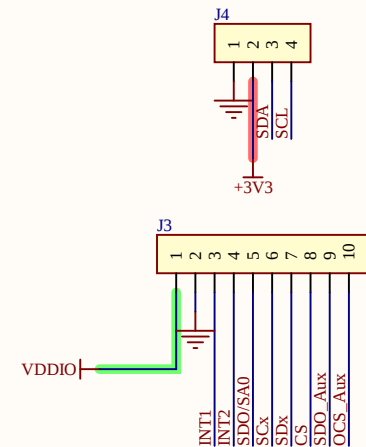
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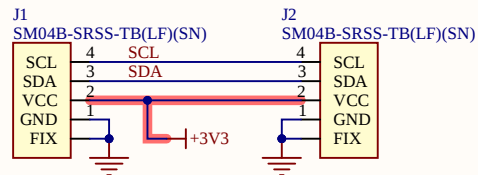


0x6A DEFAULT I2C ADDRESS

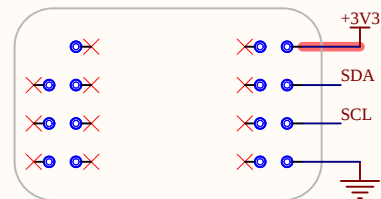
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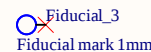
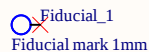
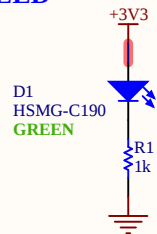
I2C CONNECTORS



TEST POINTS BOTTOM VIEW



POWER LED



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File: **TOP.SchDoc**

Version: **V0.3**

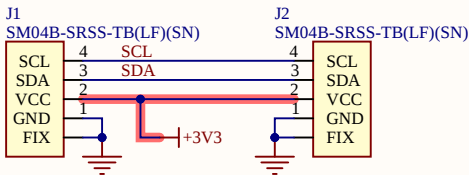
Sheet **1** of **1**

Author: **Silvio Navaretti**

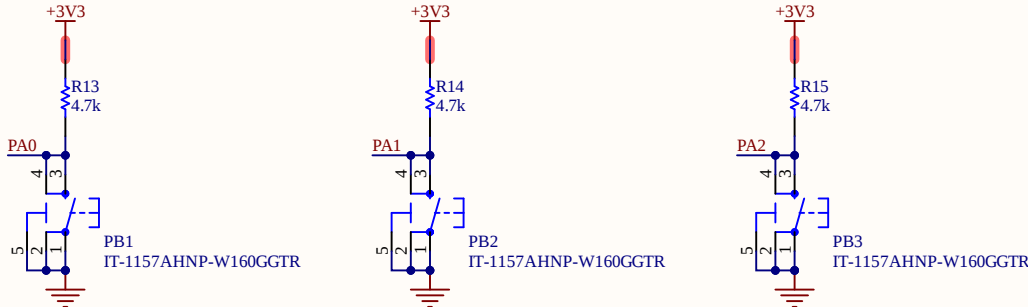
RevAuthor: **Silvio Navaretti**



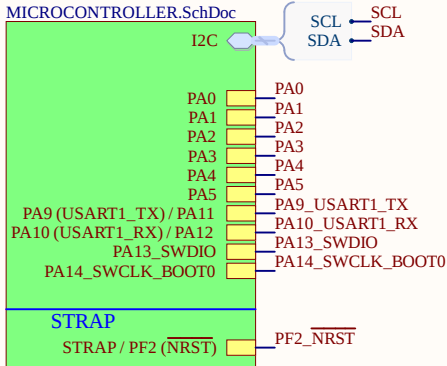
I2C CONNECTORS



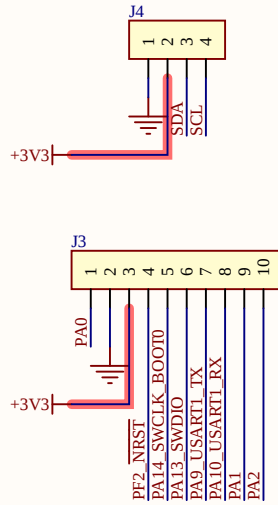
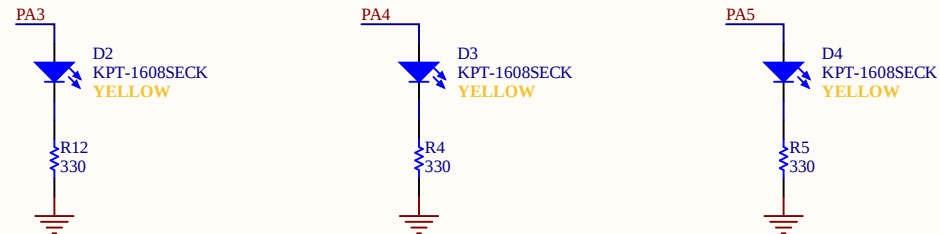
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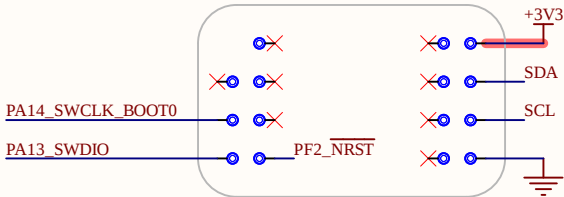
MICROCONTROLLER



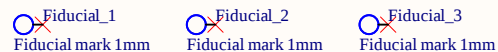
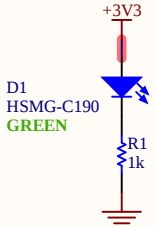
LEDs



TEST POINTS
BOTTOM VIEW



POWER
LED



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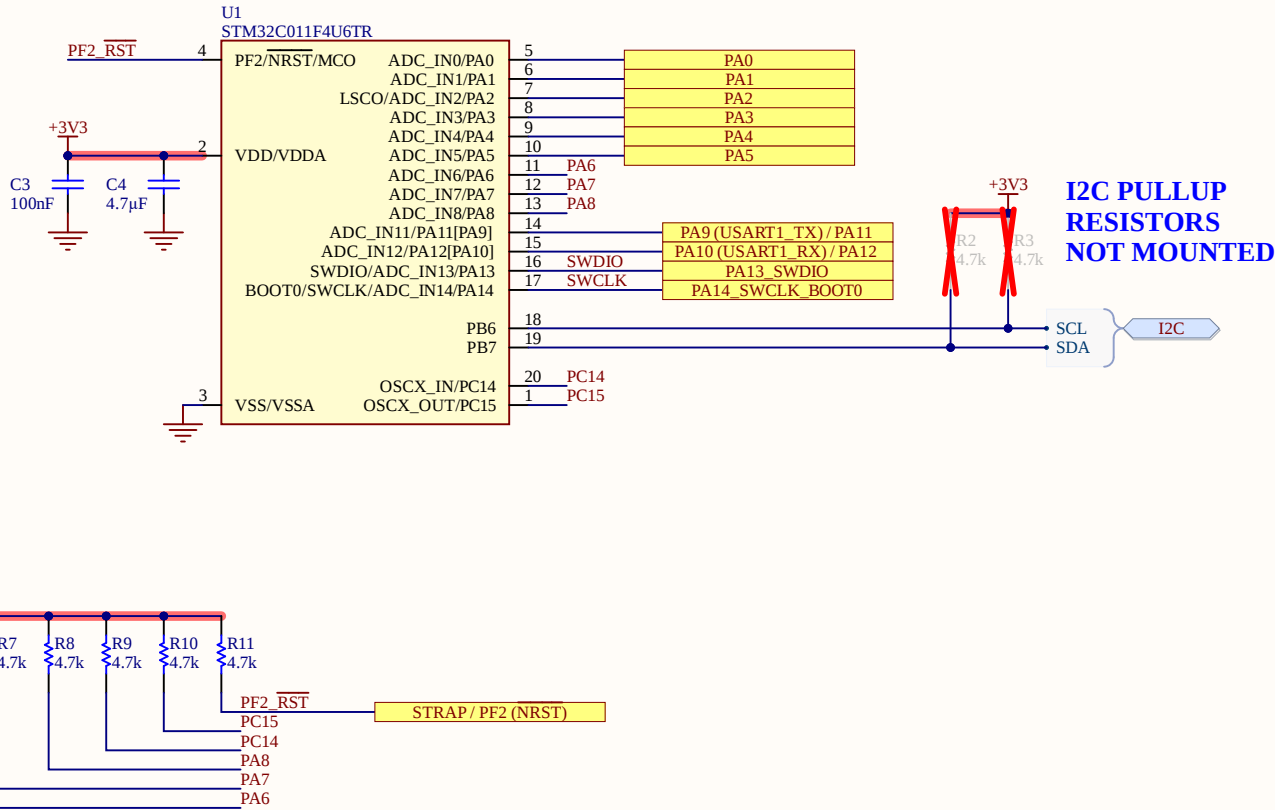
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Date: 27/06/2024	Time: 16:28:12	Sheet 1 of 2	RevAuthor: Silvio Navaretti	
File: TOP.SchDoc		Author: Silvio Navaretti		

Table 11. Terms and symbols used in Table 12		
Column	Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
I/O structure		Options for FT I/Os
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function

Table 12. Pin assignment and description

Pin	Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
20	PC14- OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
1	PC15- OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMB, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.



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ID: ABX00110

Date: 27/06/2024 Time: 16:28:13

File: MICROCONTROLLER.SchDoc

Version: V0.3

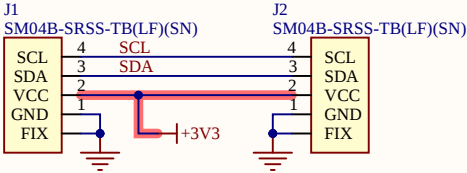
Sheet 2 of 2

Author: Silvio Navaretti

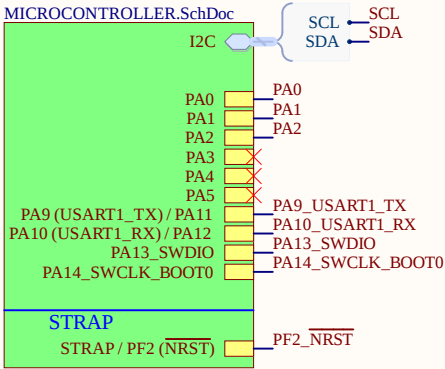
RevAuthor: Silvio Navaretti



I2C CONNECTORS

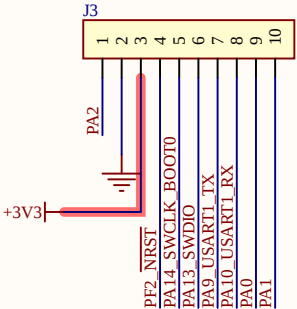
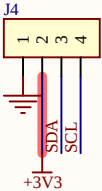
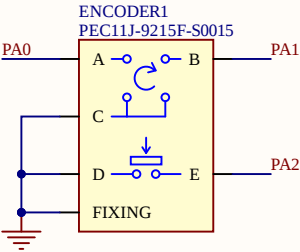


MICROCONTROLLER

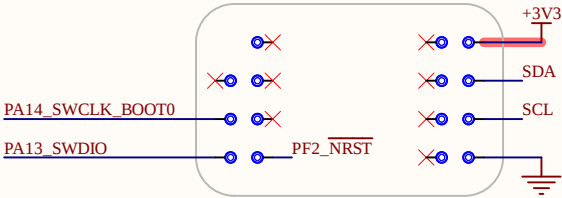


ENCODER

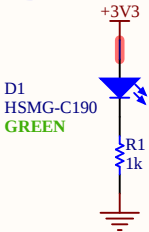
PULLUPS NOTE: Internal microcontroller pullups are enabled for encoder pin A, encoder pin B and encoder switch pin E



TEST POINTS
BOTTOM VIEW



POWER LED



QR1
QR CODE 4x4mm



Fiducial_1
Fiducial mark 1mm

Fiducial_2
Fiducial mark 1mm

Fiducial_3
Fiducial mark 1mm

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Title: TOP

ID: ABX00107

Date: 27/06/2024

File: TOP.SchDoc

Version: V0.3

Sheet 1 of 2

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

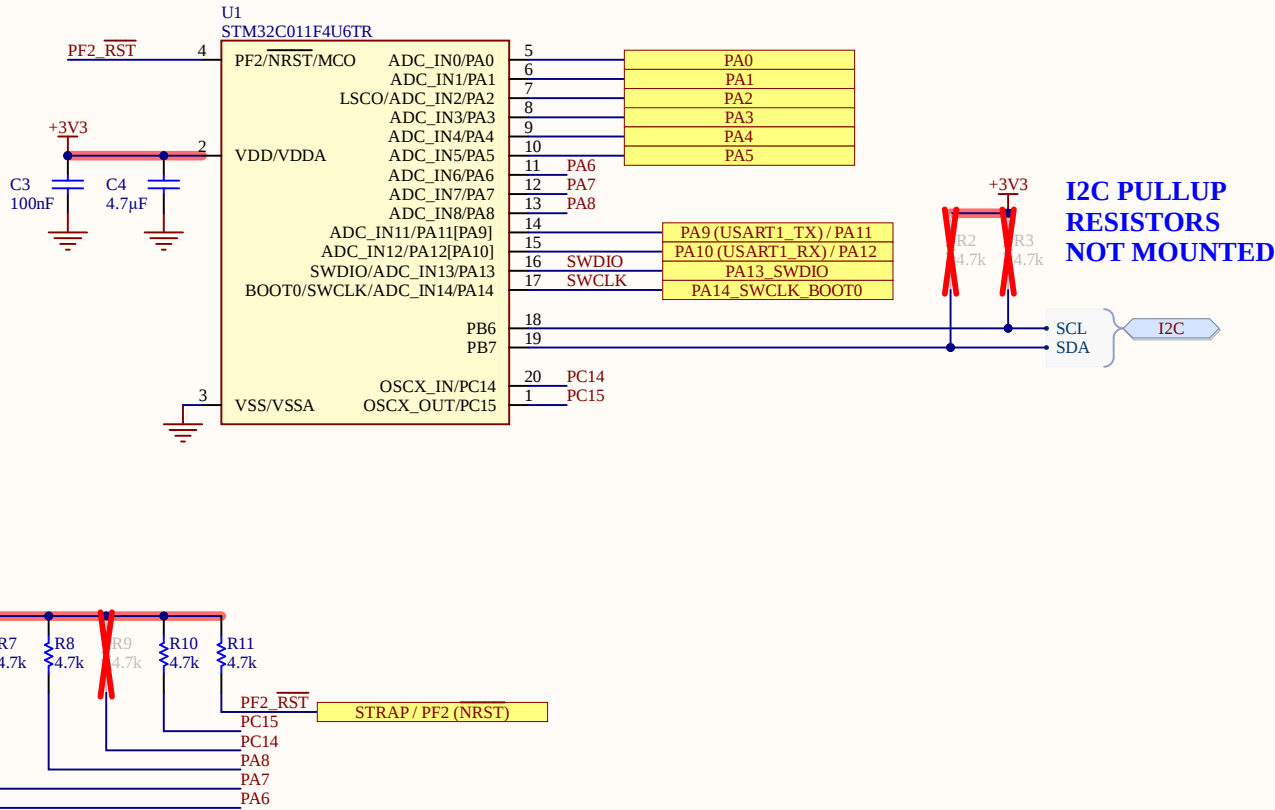


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Column	Symbol	Definition
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	_f	I/O, Fm+ capable
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Table 12. Pin assignment and description

Pin	Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
20	PC14- OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
1	PC15- OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMB, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

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Title: **Microcontroller**

ID: **ABX00107**

Date: **27/06/2024** Time: **16:19:00**

File: **MICROCONTROLLER.SchDoc**

Version: **V0.3**

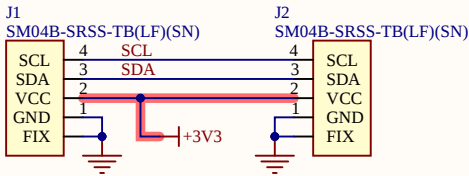
Sheet **2** of **2**

Author: **Silvio Navaretti**

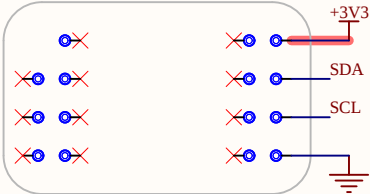
RevAuthor: **Silvio Navaretti**



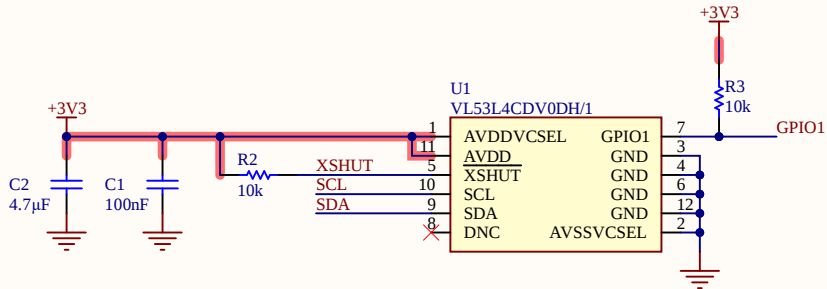
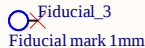
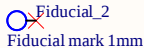
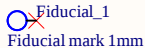
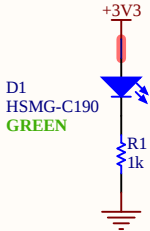
I2C CONNECTORS



TEST POINTS
BOTTOM VIEW

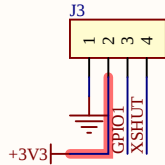
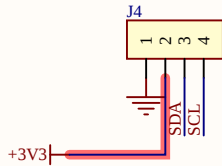


POWER LED



GPIO1 is
open drain

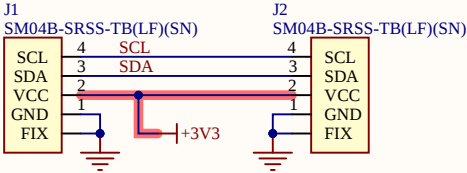
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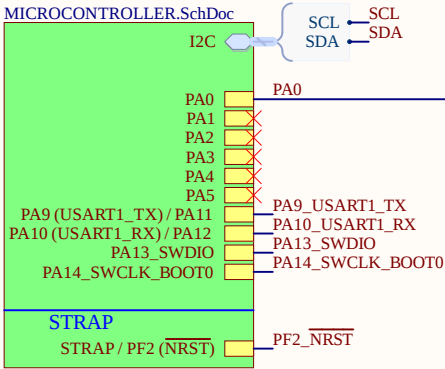
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Title: TOP		 	
ID: ABX00102	Version: V0.3		
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File: TOP.SchDoc		Author: Silvio Navaretti	

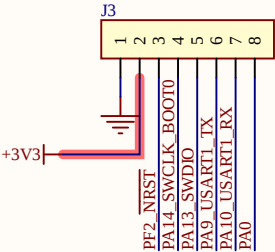
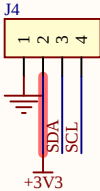
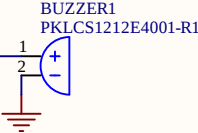
I2C CONNECTORS



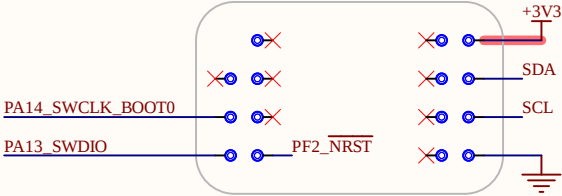
MICROCONTROLLER



BUZZER



TEST POINTS
BOTTOM VIEW



POWER LED



QR1
QR CODE 4x4mm



Fiducial_1
Fiducial mark 1mm

Fiducial_2
Fiducial mark 1mm

Fiducial_3
Fiducial mark 1mm

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Title: TOP

ID: ABX00108

Date: 27/06/2024

File: TOP.SchDoc

Version: V0.3

Sheet 1 of 2

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

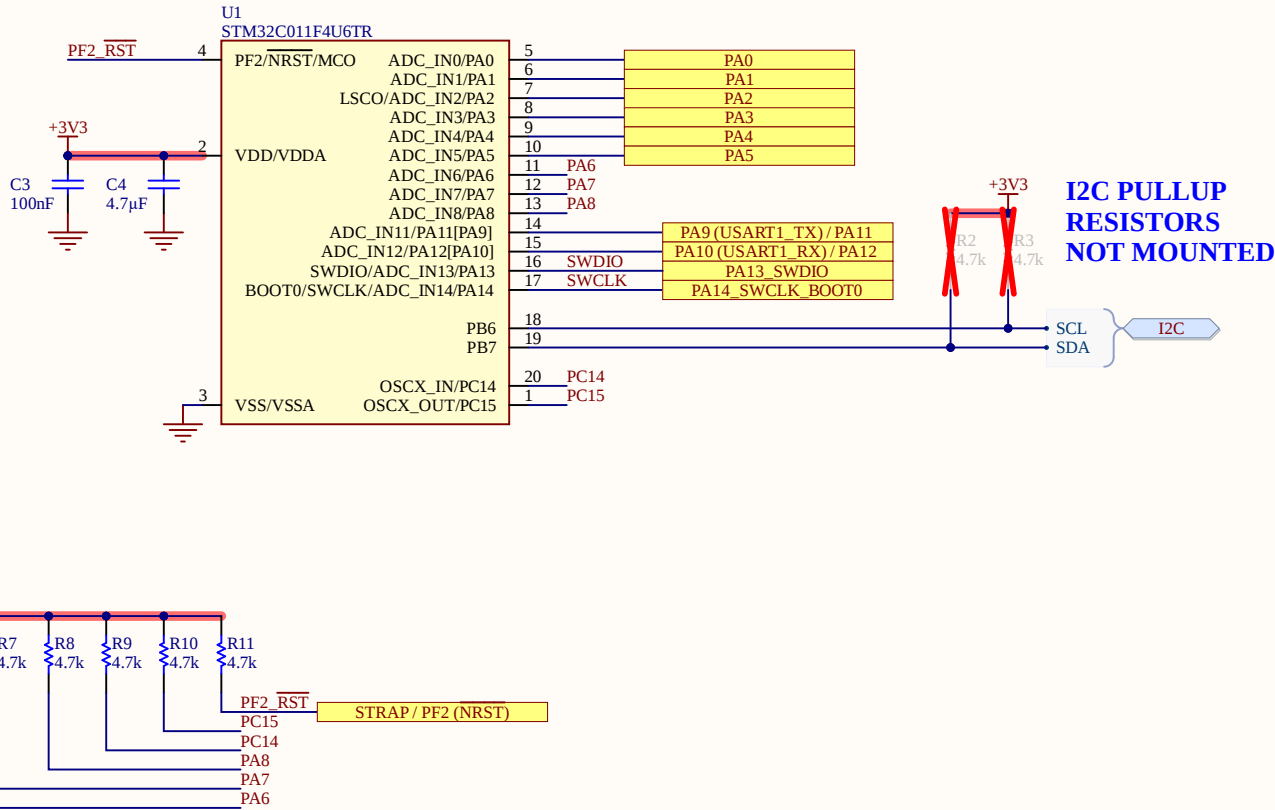


Table 11. Terms and symbols used in Table 12		
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	RST	Bidirectional reset pin with embedded weak pull-up resistor
I/O structure		Options for FT I/Os
	_f	I/O, Fm+ capable
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Table 12. Pin assignment and description

Pin	Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
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1	PC15- OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMB, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.



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Title: **Microcontroller**

ID: **ABX00108**

Date: **27/06/2024** Time: **16:22:23**

File: **MICROCONTROLLER.SchDoc**

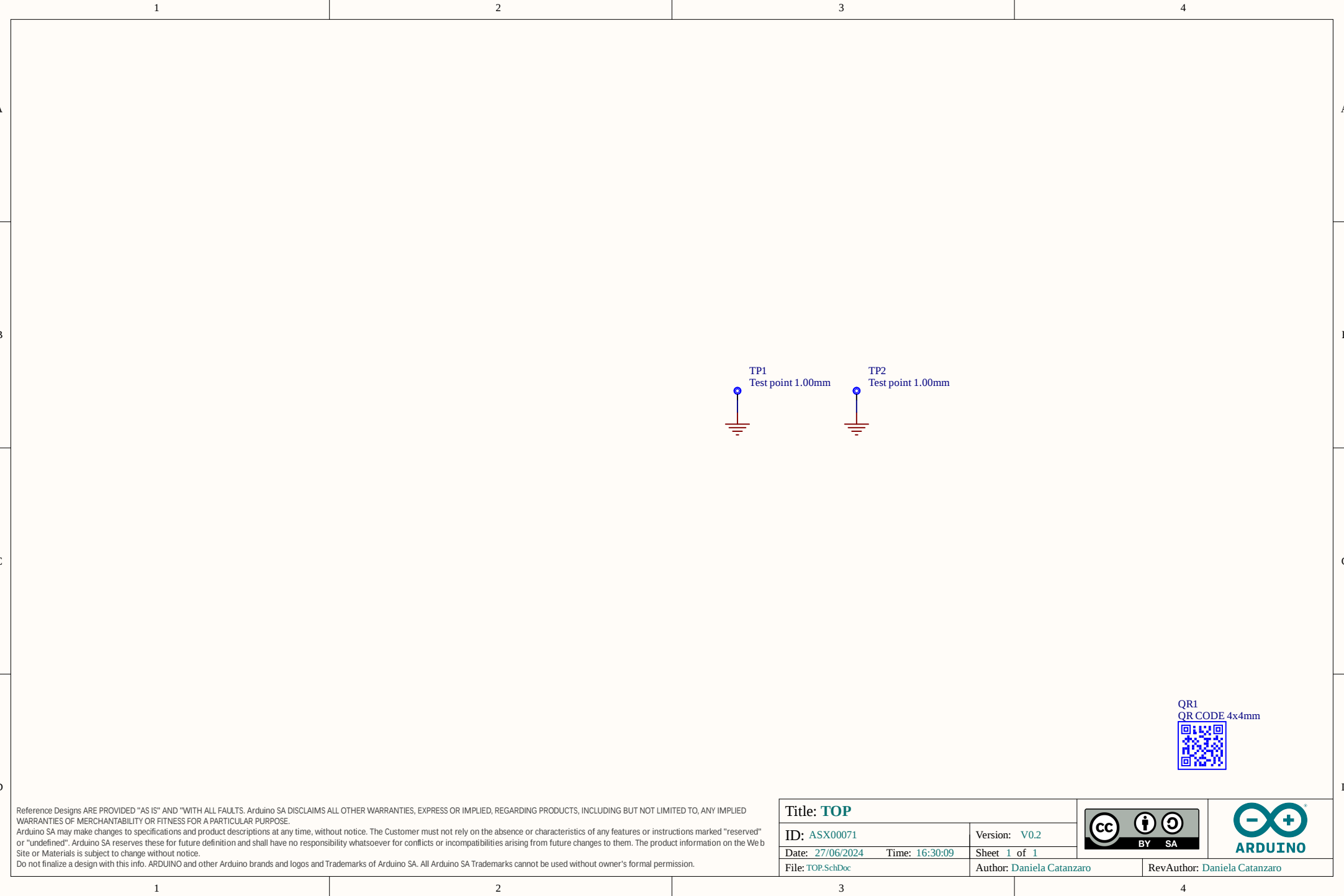
Version: **V0.3**

Sheet **2** of **2**

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